

The 17th U.S.-Korea Forum on Nanotechnology: Next-generation Semiconductors and Environmental Implications of Semiconductor Manufacturing

The Plaza Hotel, Seoul, Korea

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The first decade of the 21st century has been flourished by the advent of nanotechnology convergence and its application in a broad spectrum of science and technology areas along with interdisciplinary research initiatives to achieve rapid advancement toward 4th industrial revolution. To further promote development of new technologies, the United States (National Science Foundation, NSF) and Korea (Ministry of Science and ICT, MSIT) have been encouraging a common platform for the exchange of ideas and research collaboration in nanotechnology through these Forums, set up by the recommendations made by the Korea-US joint committee on Scientific and Technological Cooperation, held on October 31, 2002 in Seoul, Korea.

Ever since then, our Forums have been extremely successful, thriving over a decade of their organization history and promoting tremendous development in nanotechnology. These Forums have been a testimony to the transformative power of identifying a concept or trend and laying out a vision at the synergistic confluence of diverse scientific research areas. Our Forums have successfully provided a common platform for effective networking between research communities and industries in both countries by identifying emerging areas in nanotechnology which generate huge impact. This is evident from major collaboration initiatives between US and Korea, established via our Forums. Organizing the Forums has significantly expedited the generation of cutting edge technologies for the thrust areas in both countries. These Forums have been publicized through Carnegie Mellon website:

<http://www.cmu.edu/nanotechnology-forum/>.

With this mission, we established the 1st US-Korea Forum on Nanotechnology, via NSF funding, on October 14th -18th of 2003, in Seoul. As the Korean counterpart to NSF, participation was overseen and funded by MSIT. The topics in the subsequent Forums were recommended by the advisory committee members depending on the need of both countries at that time, and the locations of these Forums have alternated between Korea and the US. We organized the 2nd Forum, on nanomanufacturing research and the development of educational programs

covering the field of nanotechnology. The 3rd Forum focused on active devices and systems research, unlike the passive systems studied during the first two Forums. We held the 4th Forum, where the focus was on the sustainable nano energy with emphasis on the design and characterization of materials as well as devices and systems for energy applications. The 5th Forum focused on the emerging area of nano-biotechnology emphasizing novel nano-biomaterials, instrumentation technologies, and integrated systems for overcoming critical challenges in biomedicine and delivery of healthcare, as well as their environmental, health & safety (EHS), and toxicity issues. The 6th Forum dealt with nano-electronics with emphasis on fundamentals as well as integration with applications including convergence technology with biotechnology. The 7th Forum oversaw discussions ranging in nanotechnology convergence over current and future energy technologies to provide environmentally friendly solutions to the crippling challenges facing the energy sector. These seven Forums culminated in a seamless developmental and feedback process documenting the advent of nanotechnology convergence in broad spectrum of science and technology areas, for the first decade of the 21st century (NANO1). The 8th Forum in 2011, on nanotechnology convergence in sustainability, heralded new horizons in nanotechnology for the next decade (NANO2) by addressing critical problems faced by an ever increasing global population, with an emphasis on environmentally friendly technologies for the future on nanotechnology for sustainability, focusing on water reuse and desalination, greenhouse gas capture and conversion, and sustainable natural resources. The 9th Forum focused on channeling nanotechnology to the masses to responsibly address broad societal challenges such as nanoscience fundamentals, sustainability, and state-of-the-art applications for the new generation of nanotechnology products. The 10th Forum focused on laying out a roadmap for a new generation of nanotechnological products and processes. The 11th Forum focused on a new paradigm in nanomanufacturing, nanocomposite, and nanoinformatics. This Forum provides an opportunity to realize the potential of nanotechnology through the development of innovative and sustainable nanomanufacturing technologies for producing novel strong, light and smart nanocomposites and their management via nanoinformatics which will likely lead to paradigm shifting next generation enhanced performance of products in a broad range of existing industries including aerospace, automotive, energy, environmental remediation, information, and power industries as well as development of new industries. The 12th Forum focused on laying out a roadmap for a new paradigm in nanoscience-convergence in 2-D materials and for water purification via exploring improvements to technological tools for the application of nanotechnology and functional and novel nanomaterials to water-related topics. The 13th Forum focused on a new paradigm in nanoscience-convergence in brain-inspired (neuromorphic) computing and water & energy. The 14th Forum

focused on laying out a roadmap for a new paradigm in nanoscience-convergence including nanosensors and neuromorphic computing. The 15th Forum was focused on laying out a roadmap for a new paradigm in nanomedicine area as well as continuing effort on nanosensors including IoT devices.

The 16th Forum was held at University of California San Diego, California, USA on September 23&24, 2019, and 60 eminent scientists and policy makers in the field of nanotechnology attended. This Forum focused on realizing the promise of nanotechnology through the development of novel nanomedicine focusing on single cell level and sensors related to human cognition and brain research.

The 17th Forum explored discussions on next-generation semiconductors and environmental implications of semiconductor manufacturing. It was held at the Plaza hotel, Seoul, Korea, on April 3rd&4th, 2023, and 61 eminent scientists and policy makers in the field of semiconductor and nanotechnology attended. During this Forum, we presented three different sessions, explained below.

Session #1: During this session, we discussed the development of advanced semiconductor devices for emerging neuromorphic in-memory computing, future CMOS nodes, and monolithic 3D (M3D) integration. The development is critical in Decadal Plan for Semiconductors, introduced by keynote speaker, Dr. Zhirnov, to resolve ever-rising energy demands for information and communication technologies (ICT) versus global energy production. The innovations are well-matched with one of the Korean government's investment strategies in the nanotechnology, strengthening creative & challenging global leading nanoscience, pointed out by opening session speaker, Dr. Deok-Kee Kim. Furthermore, they are the outcomes of NNI, proposed by Dr. Roco two decades ago, where investments in nanotechnology enable novel emerging science and technology fields. In this session, four Korean and two USA researchers shared their works. Prof. Sanghun Jeon proposed an innovative negative-capacitance flash memory using a HfO₂-based reversible single-domain ferroelectric layer for high-density and energy-efficient in-memory computing applications. Prof. Towe discussed challenges and opportunities in neuromorphic computing and reviewed the development of memristors and optical synapses. He also proposed developing a neuromorphic computing framework where the details of the neuromorphic hardware can be abstracted away. Prof. Sangbum Kim presented his work for device-algorithm co-optimization for analog in-memory deep learning. His research mitigated the non-ideal properties of devices by pairing them with the optimal algorithms. Prof. Koester described the challenges and opportunities facing 2D materials for use in the future CMOS nodes, and he discussed transition-metal dichalcogenides and their potential applications for both scaled logic and memory

devices. Prof. Wooyoung Choi explained the challenges in size and power reduction in MOSFETs and presented extremely-low-power electron devices such as tunnel FETs and nanoelectromechanical devices. Prof. Sanghyeon Kim described a Ge(110)/Si(100) heterogeneous channel 3D sequential CFET as M3D integration technology, exploring thin Ge(110) surface channel p-FET by heteroepitaxy and low-temperature layer transfer.

Session #2: The session included topics of advanced packaging and heterogeneous integration with discussion on several topics like design, manufacturing, and technology aspects of advanced packaging. All the speakers emphasized that advanced packaging is going to be the crucial technology to enable the scaling of semiconductor devices. The industry is moving to advanced packaging solutions to meet the increasing data consumption and computational demand and to overcome the slowdown of Moore's law of monolithic die scaling. Several speakers from the industry elaborated on their plans to incorporate advanced packaging as their key focus of investment and R&D development.

Prof. Busnaina presented his innovative solution of scalable additive manufacturing for making electronics, including logic gates, using additive liquid-based directed assembly-based-process that does not involve etching, chemical reactions, or vacuum. It helps reduce the time and cost of electronics manufacturing by orders of magnitude. Dr. Sayoon Kang, from KMEPS, highlighted that advanced packaging can create new value beyond historic trend of cost and quality to include form factor, thermal and electrical performance. He stressed on the need for new innovations and more integration are needed for future. Dr. Jichul Kim, from Samsung, discussed that traditionally only high-performance computing (HPC) market was driving advanced packaging because of the requirement of performance and relatively low sensitivity to cost. In mobile applications, advanced packaging mostly offered low form factor which was marginal benefit only. However, with the forecast of transistor scaling slow down, introduction of advanced packaging beyond HPC is becoming a reality to provide yield improvement, design re-use and overall cost going forward. However, improving the current challenges of design lead time, system complexity and thermal issues were pointed out. Prof. Iyer, from UCLA, underlined the need for a packaging roadmap which has been missing unlike semiconductor device roadmap. He discussed the inefficiencies of current packaging schemes and presented some options to improve the power, area, latency, and bandwidth using on-chip like features for packaging applications. His analysis showed interconnect pitch of 2-10 micrometer maybe needed for advanced packaging solutions. Dr. Jiho Kang, from SK Hynix, presented their industrial focus on high bandwidth memory (HBM), and how wafer bonding using hybrid bonding is a key technology enabler for improving

capacity and performance of DRAM and memory. Dr. Zhang proposed vertical integration of industry players is important to make progress. Chiplet technology and AI applications will be key drivers for advanced packaging solutions. Dr. Donghyun Kim, from Hana Micron, expressed his concern that current closed development in OSAT and foundries does not allow for true heterogeneous integration and highlighted the need for better collaboration to bring out common standards, integration, and verification systems. Multi-chiplet package system integrity including power, thermal, electrical, and mechanical is going to be very important. Optical interconnects are also making way into being co-integrated on same package.

Overall, there are several common themes across all talks that advanced packaging is a key enabler for scaling. Fine-pitch integration, assembly, data communication, and design schemes are all active areas of research and development. Assembly, power delivery, thermal cooling, and common protocols are highlighted to be the major challenges to solve.

Session #3: This session highlighted various strategies and advancements to address the environmental impact of semiconductor manufacturing, focusing on per- and polyfluoroalkyl substances (PFAS) remediation, alternative materials, sustainable processes, and international collaboration to reduce the industry's carbon footprint and promote sustainability. Semiconductor production significantly impacts the environment, requiring vast energy and water resources, generating hazardous waste, and using concerning materials such as PFAS. Dr. Diallo discussed NSF-funded PFAS remediation work, environmental implications of semiconductor production, and industry collaboration opportunities. Perfluorocompounds (PFCs), major greenhouse gases, are used in semiconductor fabrication. Prof. Heeyeop Chae explored substituting PFCs with fluoroethers and fluoroalcohols in dielectric etching processes, reducing global warming effects by over 70%. Dr. Duran addressed Intel's environmental stewardship strategy, emphasizing research on critical materials and processes to promote industry sustainability. High global warming potentials (GWP) process gases used in plasma processing should be replaced with low-GWP alternatives to reduce emissions. Dr. Jeong Sik Lim introduced advanced measurement technologies for superior sensitivity and resolution, potentially replacing traditional monitoring methods. Prof. Handwerker stressed the need for scientists and engineers to develop sustainable materials and processes, highlighting the US CHIPS Act's role in promoting sector sustainability. Mr. Lee focused on holistic approaches to reduce carbon footprints, support eco-friendly manufacturing tools, and develop energy-efficient process solutions. Dr. Sung-Il Cho emphasized cryogenic etching technology advances as a potential solution, reducing RF power requirements and

eliminating high GWP gas needs. Prof. Philipossian introduced Flucto-CMP and slurry injection systems, two novel methods that improve CMP process performance, reduce waste, and address environmental concerns.

To explore discussions on semiconductor technology further, we intend to organize the 18th Forum on October, 2024 to be held at NSF Nano Center, USA.

The topics include two emerging themes: sensors related to human cognition and brain research as well as next-generation semiconductor. We believe that the continuation of the semiconductor area during the 18th Forum will further promote collaboration between scientists in the both countries and will identify concrete collaboration topics and teams. For the past decade, consecutive-year discussions on the same topics, which includes neuromorphic computing (13th and 14th Forums), nanosensors including IoT (14th and 15th Forums), and nanomedicine (15th and 16th Forums), had been great success. However, due to COVID-19 pandemic, we were unable to continue with this pattern. By discussing on sensors related to human cognition and brain research, we will continue our successful pattern.

The followings are detailed recommendations made by the three sessions during this Forum:

Session 1: Next-generation Semiconductor

The next-generation semiconductor 1 discussion group propose three approaches to developing collaborations between US and Korean researchers. The approaches include (1) to collaborative work on Basic Science for Nanotechnology, (2) direct PI Level Exchanges, and (3) Graduate Student Exchange Program.

In the Basic Science for Nanotechnology, we identified 4 classes of materials that include (i) 2D materials, (ii) ferroelectric RAM materials, (iii) photonic materials, and (iv) amorphous oxide semiconductor materials. We also have identified four emerging application areas that include applications in (i) 3D memory, (ii) in-memory computing, (iii) neuromorphic computing, and (iv) functional BEOL. We suggest identifying interested researchers in each combination and holding virtual workshops to encourage collaboration.

For PI-level Exchange, we suggest sharing available fabrication options in Korean and US facilities in detail and providing contact researcher information to develop collaboration. Based on the information, we create good opportunities for prototype fabrication and characterization in Korean NNFC and US NNCI. We suggest

creating a subprogram in SRC only for Korean and US companies and researchers and adopting a version of US NNCI in Korea. Also, we strongly recommend creating chances to fabricate prototypes using advanced processes of industrial companies.

For Student Exchange Program, we suggest exchanging graduate students during the summer to fabricate prototypes in the other country. We recommend using NSF IRES program to send US students to Korea while suggesting NRF develop a Korean funding program for student exchange.

Session 2: Advanced Packaging

Proposal:

1. Korea-US packaging joint research platform
 - a. Establishment of a joint platform and share status.
 - b. Establish a joint team to collaborate on additive manufacturing for Advanced Packaging (DARPA already started a program in this area NSF has not but could do the same)
 - c. Establish an advanced packaging roadmap to supplement existing roadmaps (such a MAPT) to increase the research content
 - d. Identifying specific projects supporting the roadmap
2. Establish student sponsorship
3. Establish an annual Packaging Workshop part of the major packaging conference to share the latest development from industry and academia

Part 1 Implementation

1. Korean PIs will join US PIs to propose joint projects.
 - a. Conceptual ideas for basic science to help improve packaging
2. Resourcing fab facilities across the two countries
 - a. Young scientists exchange- supplemental funds
3. Roadmap development committee. Roadmap for 3yr, 5yr, 10yr. Leverage HIR roadmap, MRHIEP, MAPT etc
4. Incentives for companies to work with Universities to support research. Industrial liaison from major companies like Samsung, Sk Hynix etc to work.
5. Supply chain challenges (getting material from vendors) could be resolved by technology (chipselets, etc.) and new R&D from industry and academia.
6. Members from industry like Samsung, SK Hynix, Apple, Intel, AMD, IBM, Meta etc to lead the effort and provide incentives. Potential Leaders from Korea- Jichul Kim, Samsung, Jiho Kang, SK Hynix, Kang Wok Lee, SK Hynix, Sayoon Kang, KMEPS, etc. Potential Leaders from US- TBD

Ideas for specific projects-

Need workshop to discuss more details on potential projects.

Some examples-

1. Prototyping
2. PDK/ADK development for conventional and additive manufacturing co
3. Design enablement
4. Power delivery and Thermal management
5. Materials for packaging
6. Integration schemes including additive manufacturing
7. End-user applications (guidance from industry)

Part 2 Implementation

1. Exchange students. Companies offer internships to students.
2. Korean students are interested in studying abroad. Sending Korean students to the US training for Korean students to exchange.
3. Special incentives for US students to study in Korea. US students may have challenges to Korea, incentivize students (free kimchi for life?).
4. Exchange ~5 students per each side (US to Korea, Korea to US)
5. Make a case that the work is related to the thesis.
6. Study abroad for PhD, master and bachelor students also.
7. Timeline: 3-month-1yr training.
8. Joint publications in flagship conferences and journals. No patents (early information sharing with members)

Part 3 Implementation

1. Leverage conferences like KSIM, ECTC, and KMEMS to have a workshop before or after for Korean-US.
2. Virtual meetings. Bilateral meetings between academics from the two countries to exchange ideas on regular basis. IP rights definition.

Governance-

Korean side NRF to manage, US side NSF to manage this (should include NIST and other agencies since they have more funds for semiconductor manufacturing than NSF)

Estimated Budget-

1. \$10 Million US dollars/ year for five years
2. With individual awards of \$500K US dollars
3. Share 50% from Korea, 50% from the US

Session 3: Environmental Implications of Semiconductor Manufacturing

The breakout team first started by aligning on some key goals that came out of

the forum discussions in this area, where we felt that the collaboration between Korea and USA could help drive innovations forward. The aligned goals are as follows:

1. Students are prepared and incorporate sustainability analysis into their future work.
2. Academic researchers are knowledgeable and incorporate sustainability into their research programs.
3. We set 1-2 specific challenges for joint Korea-USA teams to tackle together, focused on reducing use of and/or replacement of chemicals of concern.
4. We set a collective goal that programs and actions coming from the other sessions in this forum incorporate a step in which they assess the implications of their new projects on sustainable manufacturing, through the development and application of an environmental scorecard.

The team then focused on what actions and programs could be put in place to achieve the above goals, as follows:

1. Programs should be established with the USA and Korea to develop and execute short courses (coming from both academia and industry) to educate both students and researchers on real world issues and environmental implications of semiconductor manufacturing choices.
2. Set aggressive goals and fund programs to reduce (suggestion is >50% reduction in CMP chemicals for a given result) and replace (etchant gases and PFAS-containing coolants) chemicals of concern in semiconductor manufacturing.
3. There should be a joint project to develop and implement an environmental scorecard that could be used for projects moving forward to ensure environmental considerations are addressed at the onset of new projects.
4. Formally design cross-functional teams that bring in both geographic and discipline diversity to develop holistic solutions. This could be executed through a PI exchange, but could also be done via quarterly meetings where multiple geos are engaged from their home institutions.
5. We also recommend that we find a way to enable fab tours for young students to experience the immense, complex, exciting nature of semiconductor manufacturing